AD-A105 378 CORNELL UNIV ITHACA NY SCHOOL OF ELECTRICAL ENGINEERING F/G 9/1
SILICON-ON-SAPPHIRE MEDIUM POWER MESFET.(U)
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(6) Silicon-on-sapphire medium power MESFET,

The key aspect in improving the performance of SOS MESFETs is to reduce the parasitic source resistance. While the extrinsic g_m of GaAs MESFETs is now close to that of the intrinsic device (i.e., with $R_S = R_D = 0$), SOS MESFETs still have significant progress to be made in the area of source resistance reduction.

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The source resistance can be most effectively reduced by spacing the gate closer to the n^+ source implant. The smallest spacing is then determined by the gate-to-source breakdown voltage. For similar doping profiles in silicon and in GaAs we can consider the approximately universal expression for junction breakdown voltage from Sze, p. 114 et seq.

(11) Feb 81

$$V_B^* \simeq 60\left(\frac{E_g}{1.1}\right)^{3/2}\left(\frac{N_B}{10^{16}}\right)^{-3/4} \text{ volts}$$

For a cylindrical junction as expected for the MESFET gate

$$V_B \simeq V_b^*\left\{(2+\gamma)\gamma^{1/2} - \gamma\right\}$$

where

$$\gamma = \frac{r_j}{W} = \frac{\text{radius of curvature of metallurgical junction}}{\text{depletion layer width at breakdown}}$$

The maximum doping concentration is however set by the need to maintain a high gate-to-drain breakdown voltage, for example around 15V. With this breakdown voltage, a doping concentration of 6.35×10^{16} cm^{-3} is calculated. For a built in voltage of 0.8V accross the Schottky barrier gate and with a pinch-off voltage of -5V applied to the gate we get a depletion depth given by

$$W = \sqrt{\frac{2\,\epsilon_s(V_p + \phi)}{qN_D}}$$

of about 0.35 μ m. So to eliminate the possibility of space charge limited current flow between the reverse biased gate and the source, we must keep them separated by at least 0.35 μ m.

Now, typical average mobility of electrons in SOS is 400 cm^2/volt sec and in GaAs is 4000 cm^2/volt sec. So, for a 1 mm wide gate

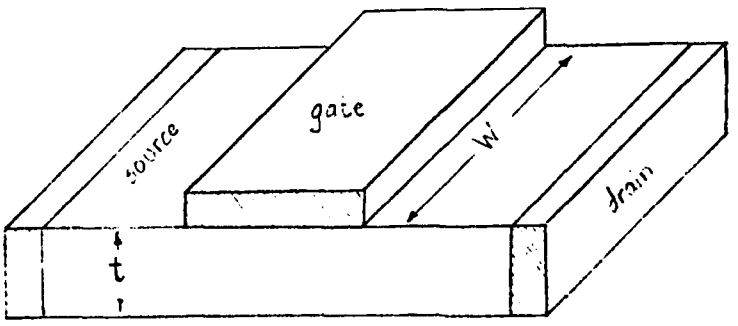
$$R^{Si} = \frac{\rho \ell}{A} = \frac{1 \times 10^{-4}}{0.35 \times 10^{-5} \times e\mu n} = 7.03\ \Omega$$

and

$$R^{GaAs} = \frac{\rho \ell}{A} = \frac{1 \times 10^{-4}}{0.35 \times 10^{-5} \times e\mu n} = 0.703\ \Omega$$

with the transfer length = 0.65 μ m. Typical transfer lengths range from 0.5 μ m to 1.5 μ m.

An illustration of the severe effects of parasitic source-gate resistance on the g_m of Si and GaAs MESFETs now follows. Consider the FET to be operating in the velocity saturation mode.



$$W = \sqrt{\frac{2\,\epsilon_s(V_p + \phi)}{q\,N_D}}$$

Now

$$I = neV(t-w)$$

$$= neVW\left(t - \sqrt{\frac{2\,\epsilon_s(V_g + \phi)}{q\,N_D}}\right)$$

but

$$g_m = \left.\frac{\partial I}{\partial V_g}\right|_{V_g=0} = 2\,\epsilon_s V\left(\frac{2\,\epsilon_s\phi}{qN_D}\right)^{-1/2} = V\left(\frac{2q\,N_D\epsilon_s}{\phi}\right)^{1/2}$$

$V_{sat} = 1 \times 10^7$ cm/sec

from which we get that since $\epsilon_{Si} \simeq \epsilon_{GaAs}$ the g_m = 164mS/mm gate width for the intrinsic device.

Now

$$g_m^{obs} = \frac{g_m^{int}}{1 + g_m^{int} R_{sg}}$$

obs = observed
int = intrinsic

For silicon,

$$g_m^{obs} = \frac{164}{1 + 7.03 \times .164} = 76 \text{ mS}$$

GaAs,

$$g_m^{obs} = \frac{164}{1 + 0.703 \times 0.164} = 147 \text{ mS}$$

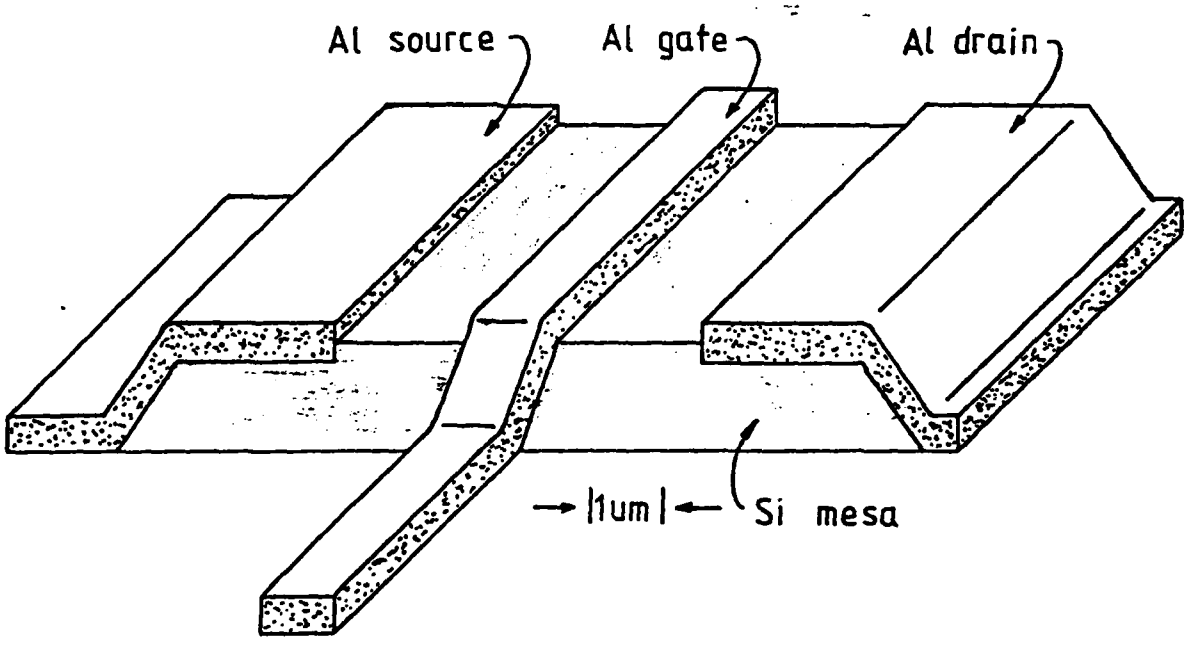
The above values have been close to what has been experimentally determined. SOS MESFETs have shown transconductances of up to 40 mS/mm and GaAs MESFETs have shown g_m's of up to 145 mS/mm at Cornell University.

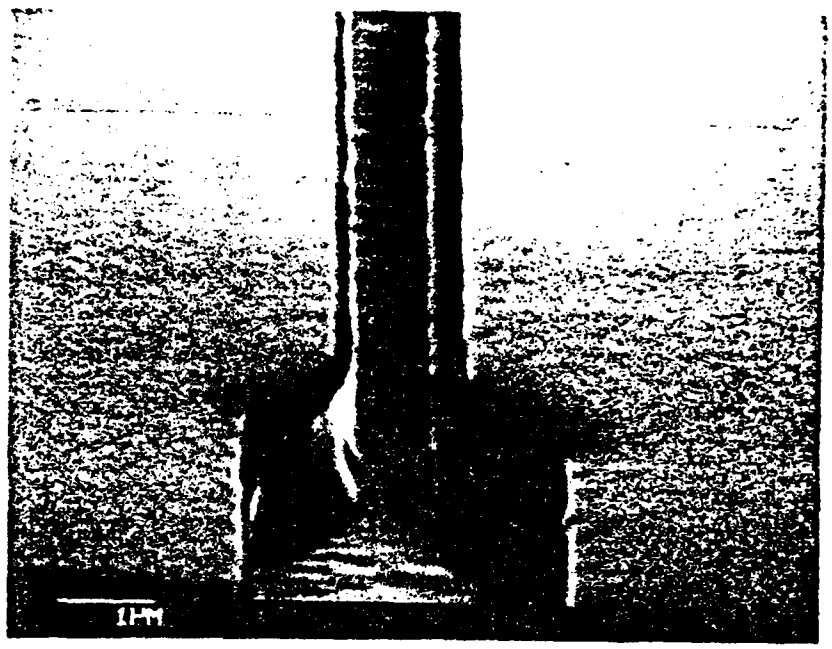
However, from practical experience with SOS MESFETs made at Cornell University, we have found that the gate breakdown voltage on SOS is larger than that predicted for pure silicon. This could be due to the high defect density in the SOS films and would allow us to increase the doping concentration for a given gate-drain breakdown voltage. The parasitic source-gate resistance would be correspondingly reduced and the extrinsic g_m comes closer to the intrinsic one. Work is in hand to determine the difference between the gate-drain breakdown voltage for devices on SOLS and bulk silicon.

A brief pictorial summary of our work on SOS MESFETs has been included to give some idea of our fabrication technology and capabilities.

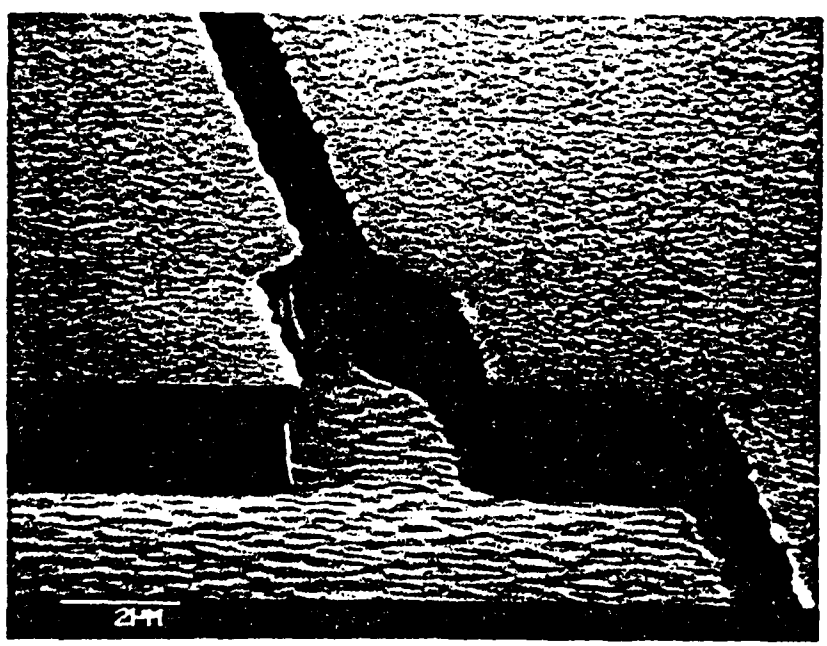
Planar SOS MESFET

- source and drain DIFFUSION or high dose IMPLANT
- MESA ion milled in argon at 500V 500nm
- channel implant 1,5E12cm^{-3} phosphorus at 120 to 160KeV
- METALLISATION 250nm Al lift off

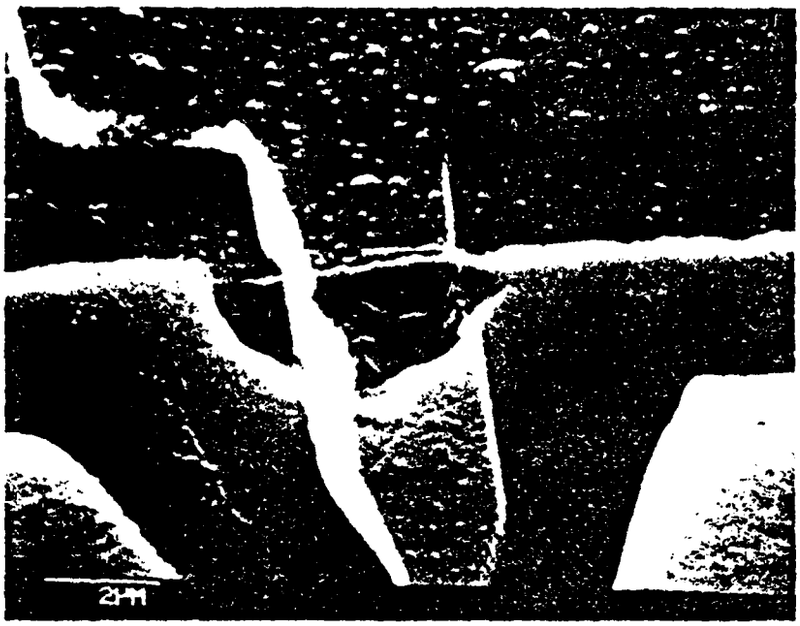


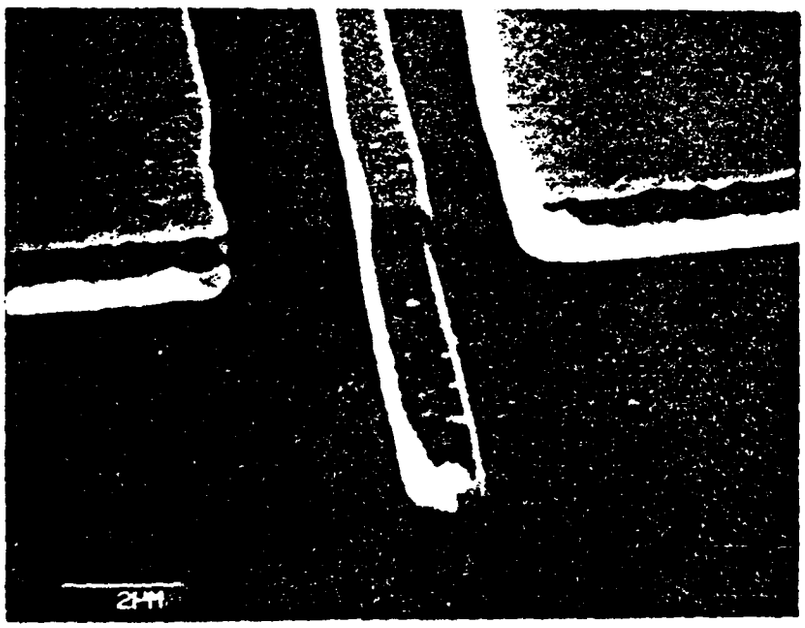


DEVELOPED GATE PATTERN IN AZ1350J

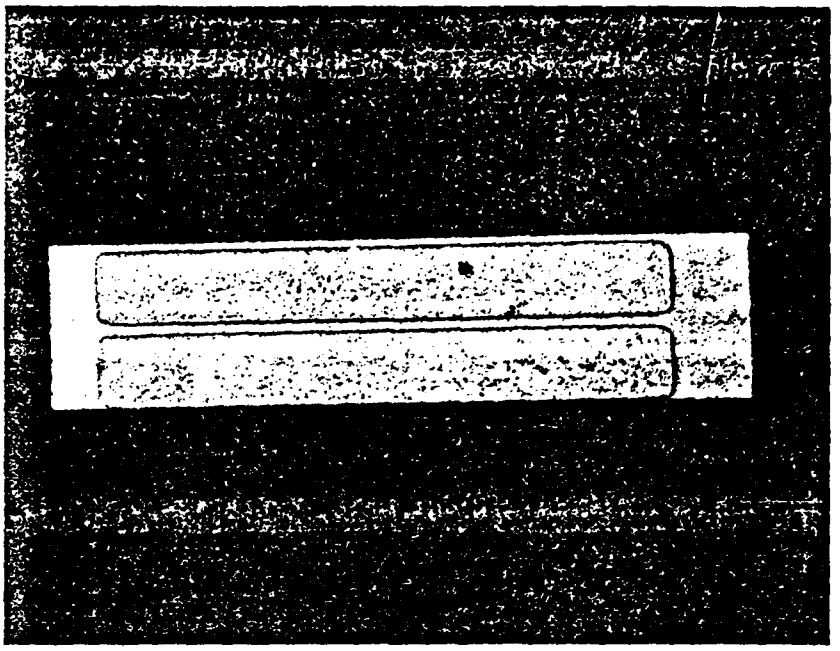


AS ABOVE BUT WITH A 2 MINUTE DIP IN TOLUENE PRIOR TO DEVELOPMENT.

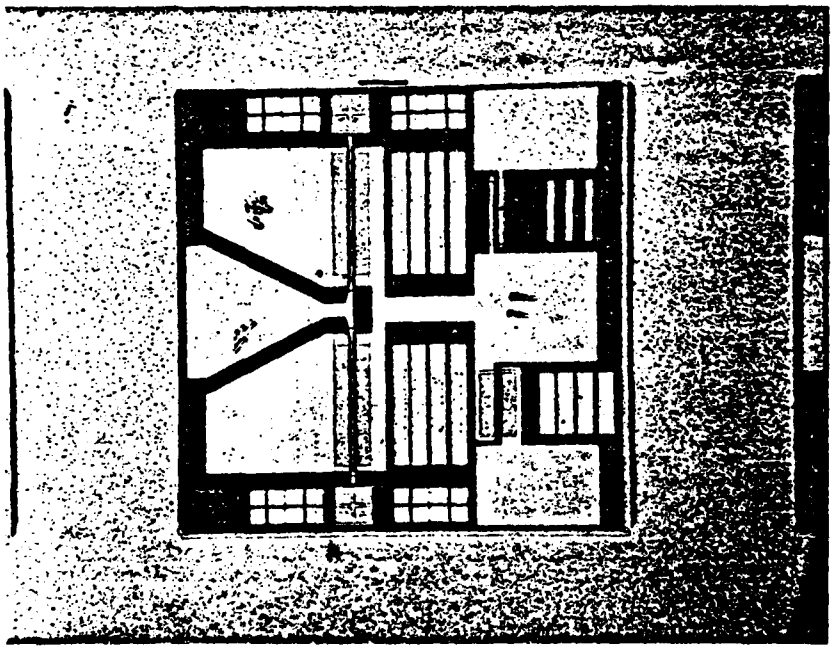




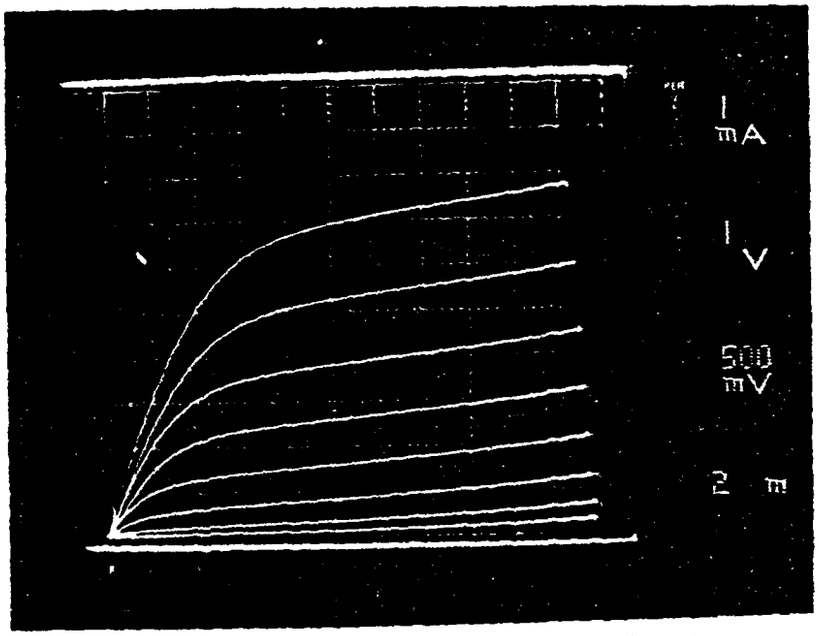
DIFFUSION OF SILICON INTO ALUMINUM.



Si Mesa with SD pattern



Final SOS MESFET

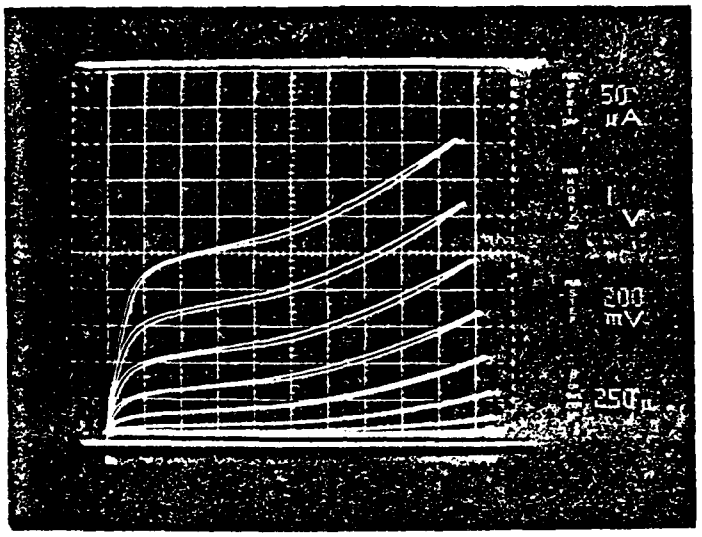


D.C. DRAIN CHARACTERISTICS FOR PLANAR-PROCESS-FET

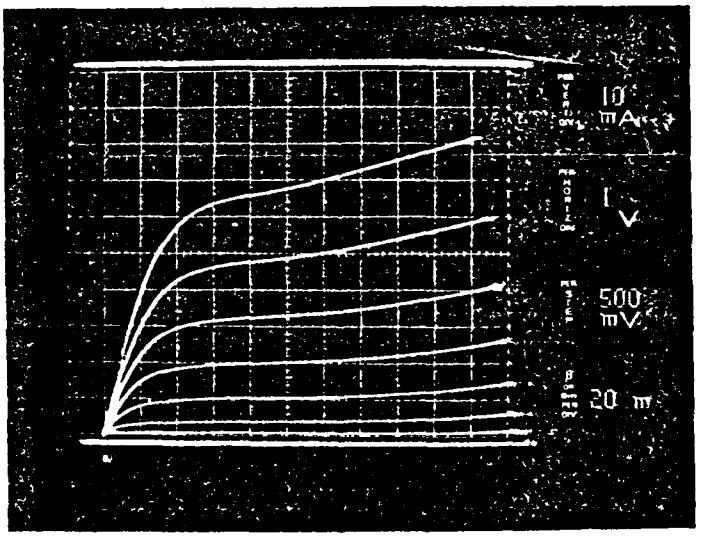
* G_M = 230 mS/cm AT V_G = 0V, V_{DS} = 5V.

* PINCH OFF VOLTAGE = - 3.8V.

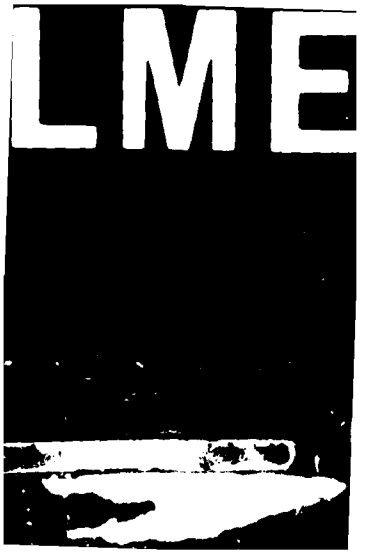
* F_T PREDICTED = 4.8 GHz.



Pt gate Lg = 1μm Wg = 40μm LSD = 3μm



Al gate Lg = 1.2μm Wg = 1.6mm LSD = 3μm


LME